

2 µA Low Dropout Positive Voltage Regulator

Features

- 2.0 µA Typical Quiescent Current
- Input Operating Voltage Range up to 10.0V
- Low Dropout Voltage:
- 250 mV (typ) @ 100 mA
- 500 mV (typ) @ 200 mA
- High Output Current: 250 mA ($V_{\text{OUT}} = 5.0V$)
- High-Accuracy Output Voltage: ±2% (max)
- Low Temperature Drift: ±100 ppm/°C (typ.)
- Excellent Line Regulation: 0.2%/V (typ.)
- Package Options: 3-Pin SOT-23A and 3-Pin SOT-89
- Short Circuit Protection
- Standard Output Voltage Options:
- 1.8V, 2.5V, 3.0V, 3.3V, 5.0V

Applications

- Battery-Powered Devices
- Battery-Powered Alarm Circuits
- Smoke Detectors
- $CO²$ Detectors
- Smart Battery Packs
- PDAs
- Low Quiescent Current Voltage Reference
- Cameras and Portable Video Equipment
- Pagers and Cellular Phones
- Solar-Powered Instruments
- Consumer Products
- Microcontroller Power

Related Literature

- AN765, "Using Microchip's Micropower LDOs", DS00765, Microchip Technology Inc., 2002
- AN766, "Pin-Compatible CMOS Upgrades to Bipolar LDOs", DS00766, Microchip Technology Inc., 2002

General Description

The MCP1701 is a family of CMOS low dropout (LDO), positive voltage regulators that can deliver up to 250 mA of current while consuming only 2.0 µA of quiescent current (typ.). The input operating range is specified up to 10V, making it ideal for lithium-ion (one or two cells), 9V alkaline and other two and three primary cell battery-powered applications.

The MCP1701 is capable of delivering 250 mA with an input-to-output voltage differential (dropout voltage) of 650 mV. The low dropout voltage extends the battery operating lifetime. It also permits high currents in small packages when operated with minimum $V_{IN} - V_{OUIT}$ differentials.

The MCP1701 has a tight tolerance output voltage regulation of ±0.5% (typ.) and very good line regulation at ±0.2%. The LDO output is stable when using only 1 µF of output capacitance of either tantalum or aluminum-electrolytic style capacitors. The MCP1701 LDO also incorporates short circuit protection to ensure maximum reliability.

Package options include the 3-pin SOT-23A and 3-pin SOT-89.

Package Types

Functional Block Diagram

Typical Application Circuits

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Electrical Specifications: Unless otherwise specified, all limits are established for an ambient temperature of $T_A = +25^\circ$ C. Parameters | Sym | Min | Typ | Max | Units | Conditions Output Voltage Regulation V_{OUT} $V_R - 2\%$ | $V_R \pm 0.5\%$ | $V_R + 2\%$ | V | $I_{OUT} = 40$ mA **([Note 1](#page-2-0))** Maximum Output Current $\begin{vmatrix} 1_{\text{OUTMAX}} & 250 \end{vmatrix}$ $\begin{vmatrix} -1 & 1 \end{vmatrix}$ mA $\begin{vmatrix} V_{\text{OUT}} & 5.0V \end{vmatrix}$ (V_{IN} = V_R + 1.0V) 200 $\sqrt{V_{OUT}} = 4.0V$ 150 $+$ $\sqrt{V_{OUT}}$ = 3.3V 150 $\sqrt{V_{\text{OUT}}}=3.0\text{V}$ 125 $\sqrt{V_{\text{OUT}}}=2.5V$ 110 $\sqrt{V_{\text{OUT}}}$ = 1.8V Load Regulation **[\(Note 3](#page-2-1))** ΔVOUT/ VOUT -1.60 ±0.8 +1.60 % VOUT = 5.0V, 1 mA ≤ IOUT ≤ 100 mA -2.25 ± 1.1 $+2.25$ $\sqrt{V_{OUT}} = 4.0V$, 1 mA $\leq I_{OUT} \leq 100$ mA -2.72 ± 1.3 $+2.72$ $\sqrt{(1.55 \times 10^{10} \text{ J/\odot} \cdot \text{s})^2} = 3.3 \times 1 \text{ mA} \leq 1.5 \times 10^{10} \text{ A}$ -3.00 \pm 1.5 +3.00 $\sqrt{(V_{\text{OUT}} = 3.0 \cdot 1 \cdot 1 \cdot 1)}$ $\sqrt{V_{\text{OUT}} = 3.0 \cdot 1 \cdot 1 \cdot 1 \cdot 1}$ -3.60 ± 1.8 $+3.60$ $\sqrt{V_{OUT}} = 2.5V, 1 \text{ mA} \leq I_{OUT} \leq 60 \text{ mA}$ -1.60 ± 0.8 $+1.60$ $\sqrt{V_{OUT}} = 1.8V, 1 \text{ mA} \leq I_{OUT} \leq 30 \text{ mA}$ Dropout Voltage V_{IN} - V_{OUT} V_{I} $+$ 400 $+$ 630 $+$ mV $|_{\text{OUT}}$ = 200 mA, V_R = 5.0V — 400 630 IOUT = 200 mA, VR = 4.0V 400 | 700 | $I_{\text{OUT}} = 160 \text{ mA}, V_R = 3.3V$ 400 | 700 | $I_{\text{OUT}} = 160 \text{ mA}, V_R = 3.0V$ 400 700 $I_{\text{OUT}} = 120 \text{ mA}, V_R = 2.5V$ — 180 300 IOUT = 20 mA, VR = 1.8V Input Quiescent Current $\begin{vmatrix} 1 & 0 \\ 0 & 1 \end{vmatrix}$ \rightarrow 1.2.0 $\begin{vmatrix} 3.0 & 4 \\ 0 & 3.0 \end{vmatrix}$ μ A $\begin{vmatrix} V_{\text{IN}} & V_{\text{R}} + 1.0V \\ V_{\text{IN}} & 1.0 \end{vmatrix}$ Line Regulation ΔV_{OUT} •100 ΔV_{IN}•V_{OUT} 0.2 $\begin{vmatrix} 0.3 \end{vmatrix}$ %/V $\begin{vmatrix} 1_{\text{OUT}} = 40 \text{ mA}, (V_R + 1) \leq V_{\text{IN}} \leq 10.0V \end{vmatrix}$ Input Voltage V_{IN} $| |$ $|$ $|$ 10 $|$ V Temperature Coefficient of Output Voltage TCV_{OUT} $+100$ $-$ ppm/° C $I_{\text{OUT}} = 40 \text{ mA}$, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ **[\(Note 2\)](#page-2-2)** Output Rise Time $\begin{array}{|c|c|c|c|c|}\hline \text{I} & \text{T}_{\mathsf{R}} & \text{I} & \text{200} & \text{I} & \text{$ $R_L = 25\Omega$ resistive

ELECTRICAL CHARACTERISTICS

1: V_R is the nominal regulator output voltage. For example: $V_R = 1.8V$, 2.5V, 3.3V, 4.0V, 5.0V. The input voltage $V_{IN} = V_R + 1.0V$, $I_{OUT} = 40$ mA.

2: TCV_{OUT} = (V_{OUT-HIGH} – V_{OUT-LOW}) *10⁶ / (V_R * ∆Temperature), V_{OUT-HIGH} = Highest voltage measured over the temperature range. $\rm V_{OUT\perp OW}$ = Lowest voltage measured over the temperature range.

3: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing.

TEMPERATURE CHARACTERISTICS

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Notes: Unless otherwise specified, $V_{OUT} = 1.8V$, 3.0V, 5.0V, $T_A = +25°C$, $C_{IN} = 1 \mu F$ Tantalum, $C_{OUT} = 1 \mu F$ Tantalum.

FIGURE 2-1: Supply Current vs. Input Voltage ($V_R = 1.8V$ *).*

FIGURE 2-2: Supply Current vs. Input Voltage ($V_R = 3.0V$ *).*

FIGURE 2-3: Supply Current vs. Input Voltage ($V_R = 5.0V$ *).*

FIGURE 2-4: Supply Current vs. Load Current (V_R *= 3.0V).*

FIGURE 2-5: Supply Current vs. Load Current (V_R *= 5.0V).*

Temperature.

FIGURE 2-6: Supply Current vs.

Note: Unless otherwise indicated, $V_{OUT} = 1.8V$, 3.0V, 5.0V, $T_A = +25^{\circ}C$, $C_{IN} = 1 \mu F$ Tantalum, $C_{OUT} = 1 \mu F$ Tantalum.

FIGURE 2-8: Output Voltage vs. Input Voltage ($V_R = 3.0V$ *).*

FIGURE 2-9: Output Voltage vs. Input Voltage ($V_R = 5.0V$ *).*

FIGURE 2-10: Output Voltage vs. Load Current (V_R *= 1.8V).*

FIGURE 2-11: Output Voltage vs. Load Current (V_R *= 3.0V).*

FIGURE 2-12: Output Voltage vs. Load Current ($V_R = 5.0V$ *).*

Note: Unless otherwise indicated, $V_{OUT} = 1.8V$, 3.0V, 5.0V, $T_A = +25^{\circ}C$, $C_{IN} = 1 \mu F$ Tantalum, $C_{OUT} = 1 \mu F$ Tantalum.

FIGURE 2-13: Dropout Voltage vs. Load Current (V_R *= 1.8V).*

FIGURE 2-14: Dropout Voltage vs. Load Current (V_R *= 3.0V).*

FIGURE 2-15: Dropout Voltage vs. Load Current ($V_R = 5.0V$ *).*

FIGURE 2-16: Start-up From V_{IN} $(V_R = 1.8V)$.

FIGURE 2-17: Start-up From V_{IN} $(V_R = 3.0V)$.

FIGURE 2-18: Start-up From V_{IN} $(V_R = 5.0V)$.

Note: Unless otherwise indicated, $V_{OUT} = 1.8V$, 3.0V, 5.0V, $T_A = +25^{\circ}C$, $C_{IN} = 1 \mu F$ Tantalum, $C_{OUT} = 1 \mu F$ Tantalum.

FIGURE 2-19: Load Regulation vs. Temperature ($V_R = 1.8V$ *).*

FIGURE 2-20: Load Regulation vs. Temperature ($V_R = 3.0V$ *).*

FIGURE 2-21: Load Regulation vs. Temperature ($V_R = 5.0V$ *).*

FIGURE 2-22: Line Regulation vs. Temperature ($V_R = 1.8V$ *).*

FIGURE 2-23: Line Regulation vs. Temperature ($V_R = 3.0V$ *).*

FIGURE 2-24: Line Regulation vs. Temperature ($V_R = 5.0V$ *).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1.](#page-8-0)

| Pin No. SOT-23A | Pin No. SOT-89 | Name | Function |
|---------------------------|--------------------------|------------------|---------------------------------|
| | | GND | Ground Terminal |
| 2 | | V_{OUT} | Regulated Voltage Output |
| ર | | V_{IN} | Unregulated Supply Input |

TABLE 3-1: PIN FUNCTION TABLE

3.1 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output and the negative side of the input capacitor. Only the LDO bias current (2 µA, typ.) flows out of this pin, there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.2 Regulated Voltage Output (V_{OUT})

Connect V_{OUT} to the positive side of the load and the positive terminal of the output capacitor. The positive side of the output capacitor should be physically located as close as possible to the LDO V_{OUT} pin. The current flowing out of this pin is equal to the DC load current.

3.3 Unregulated Supply Input (V_{IN})

Connect the input supply voltage and the positive side of the input capacitor to V_{IN} . Like all low dropout linear regulators, low source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low source impedance will depend on the proximity of the input source capacitors or battery type. The input capacitor should be physically located as close as possible to the V_{IN} pin. For most applications, 1 µF of capacitance will ensure stable operation of the LDO circuit. For applications that have load currents below 100 mA, the input capacitance requirement can be lowered. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low equivalent series resistence characteristics of the ceramic will yield better noise and PSRR performance at high frequency. The current flow into this pin is equal to the DC load current, plus the LDO bias current (2 µA, typ.).

4.0 DETAILED DESCRIPTION

The MCP1701 is a low quiescent current, precision, fixed-output voltage LDO. Unlike bipolar regulators, the MCP1701 supply current does not increase proportionally with load current.

4.1 Output Capacitor

A minimum of 1 µF output capacitor is required. The output capacitor should have an ESR greater than 0.1 $Ω$ and less than $5Ω$, plus a resonant frequency above 1 MHz. Larger output capacitors can be used to improve supply noise rejection and transient response. Care should be taken when increasing C_{OUT} to ensure that the input impedance is not high enough to cause high input impedance oscillation.

4.2 Input Capacitor

A 1 µF input capacitor is recommended for most applications when the input impedance is on the order of 10Ω. Larger input capacitance may be required for stability when operating from a battery input, or if there is a large distance from the input source to the LDO. When large values of output capacitance are used, the input capacitance should be increased to prevent high source impedance oscillations.

4.3 Overcurrent

The MCP1701 internal circuitry monitors the amount of current flowing through the P-channel pass transistor. In the event of a short circuit or excessive output current, the MCP1701 will act to limit the output current.

FIGURE 4-1: Block Diagram.

5.0 THERMAL CONSIDERATIONS

5.1 Power Dissipation

The amount of power dissipated internal to the LDO linear regulator is the sum of the power dissipation within the linear pass device (P-channel MOSFET) and the quiescent current required to bias the internal reference and error amplifier. The internal linear pass device power dissipation is calculated as shown in [Equation 5-1.](#page-10-0)

EQUATION 5-1:

 P_D (Pass Device) = $(V_{IN} - V_{OUT})$ x I_{OUT}

The internal power dissipation, as a result of the bias current for the LDO internal reference and error amplifier, is calculated as shown in [Equation 5-2](#page-10-1).

EQUATION 5-2:

 P_D (*Bias*) = V_{IN} *x* I_{GND}

The total internal power dissipation is the sum of P_D (pass device) and P_D (bias).

EQUATION 5-3:

 $P_{TOTAL} = P_D (Pass Device) + P_D (Bias)$

For the MCP1701, the internal quiescent bias current is so low (2 μ A, typ.) that the P_D (bias) term of the power dissipation equation can be ignored. The maximum power dissipation can be estimated by using the maximum input voltage and the minimum output voltage to obtain a maximum voltage differential between input and output. The next step would be to multiply the maximum voltage differential by the maximum output current.

 I_{OUTMAX}

EQUATION 5-4:

$$
P_D = (V_{INMAX} - V_{OUTMIN}) x
$$

Given:

 V_{IN} = 3.3V to 4.1V V_{OUT} = 3.0V ± 2% I_{OUT} = 1 mA to 100 mA T_{AMAY} = 55°C P_{MAX} = (4.1V – (3.0V x 0.98)) x 100 mA P_{MAX} = 116.0 milliwatts

To determine the junction temperature of the device, the thermal resistance from junction-to-ambient must be known. The 3-pin SOT-23 thermal resistance from junction-to-air (R_{0JA}) is estimated to be approximately 335° C/W. The SOT-89 R_{AIA} is estimated to be approximately 52° C/W when mounted on 1 square inch of copper. The $R_{\theta JA}$ will vary with physical layout, airflow and other application-specific conditions.

The device junction temperature is determined by calculating the junction temperature rise above ambient, then adding the rise to the ambient temperature.

EQUATION 5-5: JUNCTION TEMPERATURE – SOT-23 EXAMPLE:

 $T_J = P_{DMAX} \times R_{\theta JA} + T_A$ $T_I = 116.0$ milliwatts \times 335°C/W + 55°C $T_I = 93.9$ °C

EQUATION 5-6: JUNCTION TEMPERATURE – SOT-89 EXAMPLE:

 $T_I = 116.0$ milliwatts \times 52°C/W + 55°C

 $T_J = 6I^{\circ}C$

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

 $\mathfrak D$ represents first voltage digit 1V, 2V, 3V, 4V, 5V, 6V

Ex: $3.xV = 3000$

2 represents first decimal place voltage (x.0 - x.9)

Ex: $3.4V = \textcircled{3} \oplus \textcircled{1}$

3 represents polarity

 $0 =$ Positive (fixed)

4 represents assembly lot number

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

EIAJ SC-59 Equivalent

Drawing No. C04-104

3-Lead Plastic Small Outline Transistor (MB) (SOT89)

*Controlling Parameter

Notes:

exceed .005" (0.127mm) per side. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not

JEDEC Equivalent: TO-243

Drawing No. C04-29

APPENDIX A: REVISION HISTORY

Revision B (May 2005)

The following is the list of modifications:

- 1. Removed T0-92 device from entire data sheet.
- 2. Added Appendix A: Revision History.

Revision A (March 2004)

• Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

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NOTES:

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